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## The effect of device geometry and crystal orientation on the stress-dependent offset voltage of 3C–SiC(100) four terminal devices†

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**This communication reports for the first time, the impact of device geometry on the stress-dependent offset voltage of single crystal p-type 3C–SiC four terminal devices. Single crystal p-type 3C–SiC(100) was grown by low pressure chemical vapor deposition and three different device geometries (cross, rectangle and square) were fabricated using the conventional photolithography and dry etching processes. It was observed that the stress-dependent offset voltage of the devices strongly depends upon the device geometry and it can be increased by almost 100% by just selecting the appropriate device geometry. We also found that as the device is rotated within the (100) crystal plane its stress sensitivity varies from  $\approx 0$  to  $9 \times 10^{-11} \text{ Pa}^{-1}$ .**

Silicon carbide (SiC) with its excellent electrical and thermo-physical properties has attracted attention in recent years for stress sensing applications in harsh environments.<sup>1–3</sup> A large number of studies have been carried out by many researchers on various polytypes of single crystalline SiC such as 3C–SiC, 4H–SiC, and 6H–SiC. Experimental and theoretical results reported in the literature have proved that SiC shows high potential for stress sensing applications in harsh environments.<sup>4–13</sup> There are over 200 polytypes of SiC and only a few of them are established in the semiconductor industry including 4H–SiC, 6H–SiC and 3C–SiC. Among these polytypes 3C–SiC is more cost-effective and is compatible with the existing MEMS technology because it can be readily grown on Si wafers due to its capability for hetero-epitaxial growth on Si substrates.<sup>14–16</sup>

Most of the previous work on the piezoresistive effect in SiC has been focused on the two terminal resistor, which normally suffers from several drawbacks. Diffused and implanted resistors have the drawback of high-temperature sensitivity relative to the stress response.<sup>17,18</sup> For an accurate measurement of stress, great

care must be exercised and a Wheatstone bridge and/or amplifier is mandatory to provide an easily detectable signal. The use of Wheatstone bridge leads to several drawbacks. As such, the four resistors in the bridge must be closely matched to obtain zero offset. Additionally, these four resistors must also have almost the same temperature coefficient to avoid a significant change in the zero offset due to temperatures.<sup>18–21</sup> To increase the total resistance, two terminal resistors are designed with relatively large meandering patterns, but they suffer from transverse sensitivity which is difficult to estimate due to the lateral diffusion that occurs during the fabrication process.<sup>18</sup> Four-terminal devices (often referred to as van der Pauw devices, Hall devices, pseudo-Hall devices) have been proven to overcome the drawbacks of two terminal resistors, being more thermally stable as it does not rely on any external Wheatstone bridge and can be made as small as possible.<sup>18–22</sup> Kanda *et al.* found that the offset voltage of silicon based four-terminal devices without a magnetic field is very sensitive to mechanical strain and it depends upon the shape and orientation of the device in the crystal plane.<sup>19,23–27</sup> Since then, a large number of studies on the offset voltage dependence of the four-terminal devices has been carried out,<sup>18–21,28</sup> and in fact, the effect has been utilized commercially in pressure sensors and force sensors.<sup>29,30</sup>

To the best of our knowledge, until now, there has been no report on the effect of device geometry for single crystal p-type 3C–SiC based four terminal devices. Therefore, this communication aims to investigate the influence of device geometry on the stress-dependent offset voltage of p-type 3C–SiC four terminal devices in the (100) crystal plane. The insight achieved in this study provides a fundamental knowledge for choosing the appropriate device geometry with an optimized input current direction in the (100) crystal plane for designing 3C–SiC MEMS mechanical sensors. Also the preferred device geometry in the (100) crystal plane can be predicted for magnetic field sensors to minimize the offset voltage variations due to various stresses.

P-type 3C–SiC was grown on a Si(100) substrate by low pressure chemical vapor deposition in which SiH<sub>4</sub> and C<sub>2</sub>H<sub>2</sub> were employed

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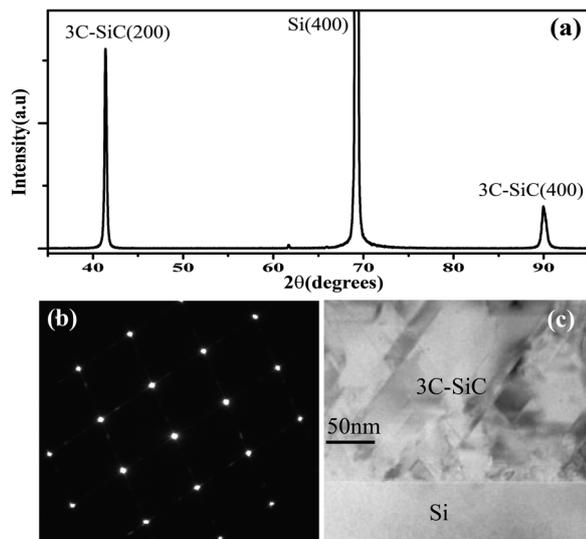


Fig. 1 (a) The XRD pattern of 3C-SiC grown on Si(100); (b) the SAED image of 3C-SiC; (c) the TEM image of 3C-SiC. Reproduced with permission from ref. 5. Copyright[2014], AIP Publishing LLC.

as the precursors. The *in situ* doping of the 3C-SiC film was performed using trimethylaluminium (TMAI) precursor as the source of the Al (p-type) dopant. The quality of the SiC film was investigated by X-ray diffraction analysis (Fig. 1(a), selected area electron diffraction (SAED in Fig. 1(b)) and transmission electron microscopy (Fig. 1(c)). Epitaxial 3C-SiC thin films of good crystalline quality were confirmed using these techniques (see the ESI†).<sup>31</sup> The electrical properties of the grown film were characterized using Hall effect measurements. The carrier concentration of the p-type single crystalline 3C-SiC was found to be approximately  $5 \times 10^{18} \text{ cm}^{-3}$ , while the carrier concentration of the Si substrate was  $5 \times 10^{14} \text{ cm}^{-3}$ . The resistivity of the SiC thin film was measured using the four point probe method and was found to be  $0.14 \Omega \text{ cm}$  and thus the hole mobility of the single crystalline 3C-SiC thin film was calculated to be  $9 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ .<sup>5</sup> Three different geometries of four terminal devices including rectangle, square and cross were fabricated in three different orientations using conventional photolithography and dry etching processes (Fig. 2). The devices were fabricated in three different orientations by rotating the mask during photolithography process with respect to the reference orientation of the wafer (see the ESI†). Aluminium was used for depositing Ohmic contacts to the device. After fabrication of the device, the wafer was diced into strips of dimensions  $60 \text{ mm} \times 9 \text{ mm} \times 0.625 \text{ mm}$  to apply strain using the bending beam method.<sup>6</sup>

To investigate the effect of stress on the fabricated devices the strain was induced into the devices using bending beam method in which one end of the Si beam with 3C-SiC four terminal devices was fixed, while the other end was bent by attaching different loads. The bi-layer model has been used to calculate the strain induced into 3C-SiC devices on the Si beam (see the ESI†). The method to numerically calculate the strain and stress induced into the SiC layer on the Si strip is reported elsewhere.<sup>6</sup>

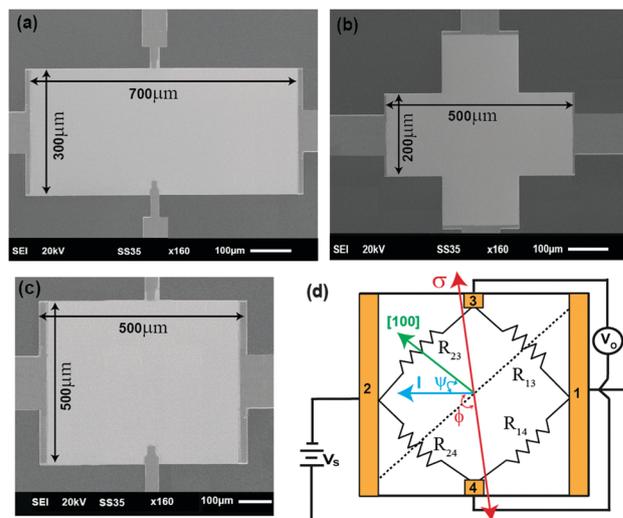


Fig. 2 SEM images of the fabricated devices: (a) rectangular device, (b) cross-device, (c) square device (d) equivalent circuit model of the square device for theoretical calculations:  $\psi$  is the angle between the direction of current and the [100] crystal orientation,  $\phi$  is the angle between the direction of stress and the direction of current.

Accordingly, the compressive and tensile stress applied to the SiC layer was in the range of  $-264 \text{ MPa}$  to  $264 \text{ MPa}$ . As 3C-SiC is grown on Si, the leakage current through the SiC/Si heterojunction was investigated and it was found that the large valence band offset between Si and SiC ( $1.7 \text{ eV}$ ) prevents the leakage of current through the SiC/Si junction. The leakage current was measured to be only 0.1% of the total current flowing through the fabricated devices.<sup>32–34</sup> Fig. 2(d) shows the equivalent circuit diagram for the square device. The input signal is applied between terminals 1 and 2 while the output voltage is measured at terminals 3 and 4. When stress is applied to the device at constant input current, an output voltage is observed at terminals 3 and 4 which increases linearly with the increase of the applied stress.

Fig. 3 shows the ratio of the output voltage to the input voltage of the cross-device at different stress and current directions in the

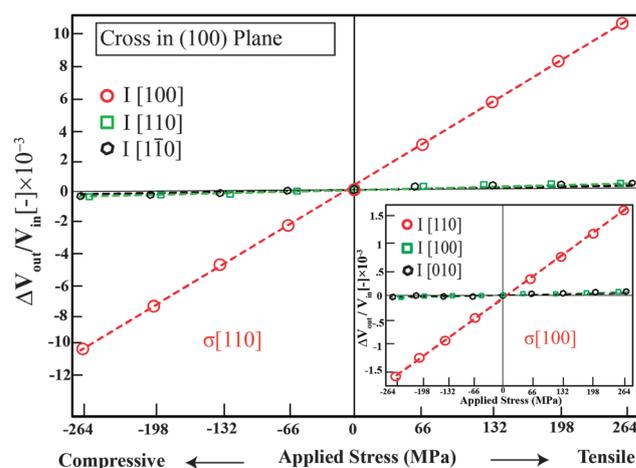


Fig. 3 The ratio of output voltage to the input voltage of cross device in (100) plane with varying stress in [110] direction. The inset shows ratio of output voltage to the input voltage with varying stress in [100] direction.

(100) crystal plane. It can be observed from Fig. 3 that the ratio of the output voltage to the input voltage for the cross-device shows a smooth linear behavior to the applied compressive and tensile stresses and it varies significantly as the direction of device current is rotated in the (100) crystal plane. We have examined the device behavior at three different directions of applied current in the (100) plane as shown in Fig. 3. The device has the highest possible sensitivity when the current is in the [100] direction and the applied stress is in the [110] direction. The minimum possible output signal with applied stress is observed when the current is in the [010] direction and the stress is in the [100] direction. So the ratio of the output signal to the input signal per unit stress in the (100) crystal plane varies from  $\approx 0$  to  $9 \times 10^{-11} \text{ Pa}^{-1}$  as the direction of input current is varied in the (100) crystal plane.

Fig. 4 shows the ratio of the output voltage to the input voltage of the rectangular device for different directions of applied stress and current in the (100) plane. It can be observed from Fig. 4 that the ratio of the output voltage to the input voltage of the rectangular device also shows a smooth linear behavior to the applied compressive and tensile stresses; in addition its value is slightly larger than that of the cross-device. Upon the rotation of the device in the crystal plane similar behavior is observed and the directions of current and stress for highest and lowest output signal are also the same as that of the cross-device. Fig. 5 shows the ratio of the output voltage to the input voltage of the square device for different directions of current and stress in the (100) crystal plane. The ratio of the output voltage to the input voltage for the square device has a much larger value (100% large) as compared to both the cross- and rectangular devices. The directions of highest and lowest output voltage against stress are the same as those of cross- and rectangular devices. Fig. 6 shows the comparison of all the geometries for maximum output voltage produced when stress is in the [110] direction and the current is in the [100] direction and *vice versa* in the inset. From the comparison of the devices it is deduced that the output voltage produced due to stress by the square geometry is increased by 100% as compared to those of cross- and rectangular

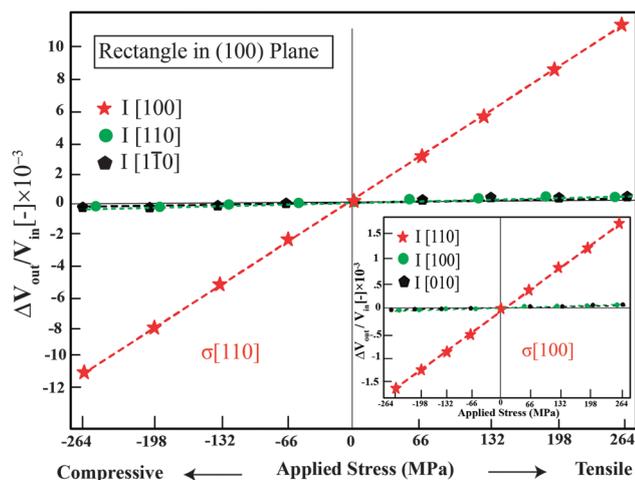


Fig. 4 The ratio of output voltage to the input voltage of rectangular device in (100) plane with varying stress in [110] direction. The inset shows ratio of output voltage to the input voltage with varying stress in [100] direction.

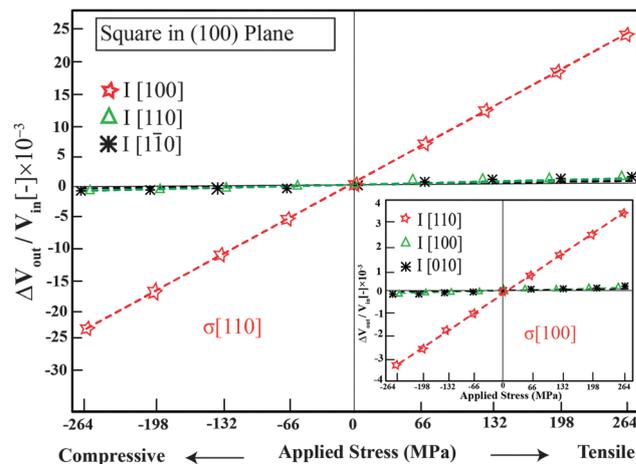


Fig. 5 The ratio of output voltage to the input voltage of a square device in the (100) plane with varying stress in the [110] direction. The inset shows the ratio of output voltage to the input voltage with varying stress in the [100] direction.

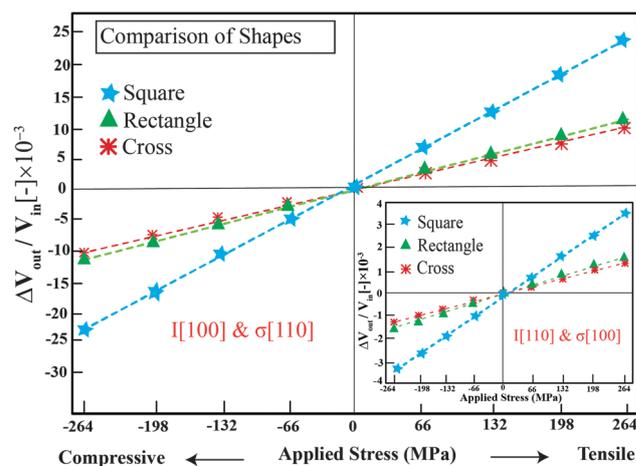


Fig. 6 Comparison of all shapes in the directions of maximum stress output voltage against stress.

geometries. In order to quantitatively explain the influence of stress on the offset voltage of these different geometries of 3C-SiC four terminal devices, a model has been used to explain the stress response of the devices.<sup>24</sup> From the equivalent circuit shown in Fig. 2(d), the offset voltage  $V_o$  can be presented using a square type bridge circuit consisting of  $R_{13}$ ,  $R_{14}$ ,  $R_{23}$  and  $R_{24}$ ; and without stress  $R_{13} = R_{14} = R_{23} = R_{24} = R_{in}$ , where  $R_{in}$  is the initial resistance without stress). The output voltage of the device is given by:

$$V_o = \frac{(R_{13}R_{24} - R_{14}R_{23})V_{in}}{(R_{14} + R_{24})(R_{13} + R_{23})}f(w, l) \quad (1)$$

where  $f(w, l)$  is a function of length and width of the device with ( $w \leq l$ ) and is given by the following equation:<sup>23,26</sup>

$$f(w, l) = \frac{1}{\left(3 - 2\frac{w}{l}\right)} \quad (2)$$

For a square device  $f(w, l) = 1$ , as  $w = l = 500 \mu\text{m}$ . In the case of a rectangular device,  $f(w, l) = 1/2.14$ , as  $w = 300 \mu\text{m}$  and  $l = 700 \mu\text{m}$ .

Similarly, for the cross-device we have  $f(w,l) = 1/2.2$  with the dimensions  $w = 200 \mu\text{m}$ ,  $l = 500 \mu\text{m}$ . These geometrical factors are introduced due to the additional input resistance for rectangular and cross-geometries as compared to the symmetrical square device.<sup>24</sup> Due to the symmetry of the square device we consider the square device as a general case and use the results to explain the results in other devices. So, when a tensile stress is applied to the square device, for example in the [110] orientation, the resistors  $R_{14}$  and  $R_{23}$  are stressed in the longitudinal direction, whereas resistors  $R_{13}$  and  $R_{24}$  are stressed in the transverse direction, leading to a change in the symmetry of the device. This results in a shift of the offset voltage  $V_o$ .

The change of the resistance under stress  $\sigma$  is:<sup>23</sup>

$$\begin{cases} R_{13} = R_{24} = R_{in} [1 + (\pi_l \cos^2 \omega + \pi_t \sin^2 \omega) \sigma] \\ R_{23} = R_{14} = R_{in} [1 + (\pi_t \cos^2 \omega + \pi_l \sin^2 \omega) \sigma] \end{cases} \quad (3)$$

where  $\pi_l$  and  $\pi_t$  are longitudinal and transverse piezoresistive coefficients of 3C-SiC in the direction of applied current and  $\omega = \phi + 45^\circ$  is the angle between the direction of stress and the diagonal of the device indicated by the dotted line in Fig. 2(d). Here  $\phi$  is the angle between direction of current and stress. From eqn (1) and (3), the generated output voltage ( $V_o$ ) at terminals 3 and 4 when applying input voltage ( $V_{in}$ ) at terminals 1 and 2 is calculated as:

$$V_o = \frac{(\cos^2 \omega - \sin^2 \omega)(\pi_l - \pi_t)\sigma V_{in} f(w,l)}{2} \quad (4)$$

Thus, the ratio of the output voltage generated at terminals 3 and 4 to the input voltage is:

$$\frac{V_o}{V_{in}} = \frac{(\cos^2 \omega - \sin^2 \omega)(\pi_l - \pi_t)\sigma}{2} f(w,l) \quad (5)$$

The values of longitudinal and transverse piezoresistive coefficients  $\pi_l$  and  $\pi_t$  depend upon the direction of applied stress. In order to theoretically analyze the offset voltage  $V_o$ , the values of  $\pi_l$  and  $\pi_t$  are taken from ref. 5 and can be written as:

$$\begin{cases} \pi_l = \pi_{11} - \frac{1}{2}(\pi_{11} - \pi_{12} - \pi_{44}) \sin^2 2\Psi \\ \pi_t = \pi_{12} + \frac{1}{2}(\pi_{11} - \pi_{12} - \pi_{44}) \sin^2 2\Psi \end{cases} \quad (6)$$

where  $\pi_{11}$ ,  $\pi_{12}$  and  $\pi_{44}$  are fundamental piezoresistive coefficients of p-type 3C-SiC and  $\Psi$  is the angle between the applied current and the [100] orientation in the (100) plane. Fig. 7 shows the comparison of experimental and modeled values of the ratio of the output voltage to the input voltage of all the devices when stress is in the [110] direction and current is in the [100] direction and *vice versa*. It can be observed that the modeled and experimental values are in good agreement with an error less than  $\pm 5\%$ . Similarly, the model is valid for all other directional combinations of current and stress. We define the sensitivity ( $S$ ) of the device as:

$$\text{Sensitivity} = S = \frac{V_o}{\sigma V_{in}} \quad (7)$$

Fig. 8 shows the comparison of sensitivities of all the fabricated devices with the variation of current and stress directions

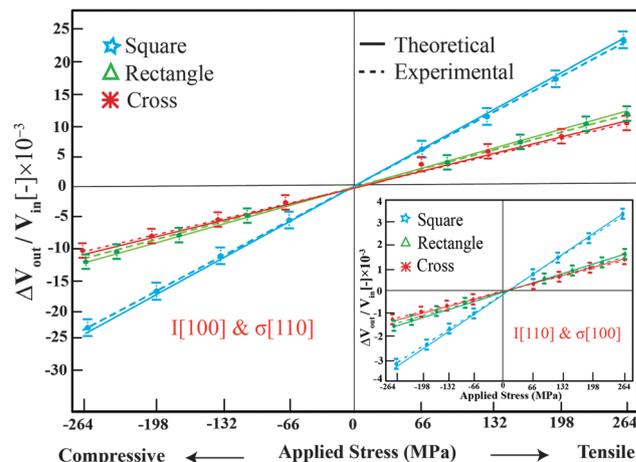


Fig. 7 Comparison of experimental and modeled values of the ratio of output voltage to the input voltage for all device geometries for maximum output.

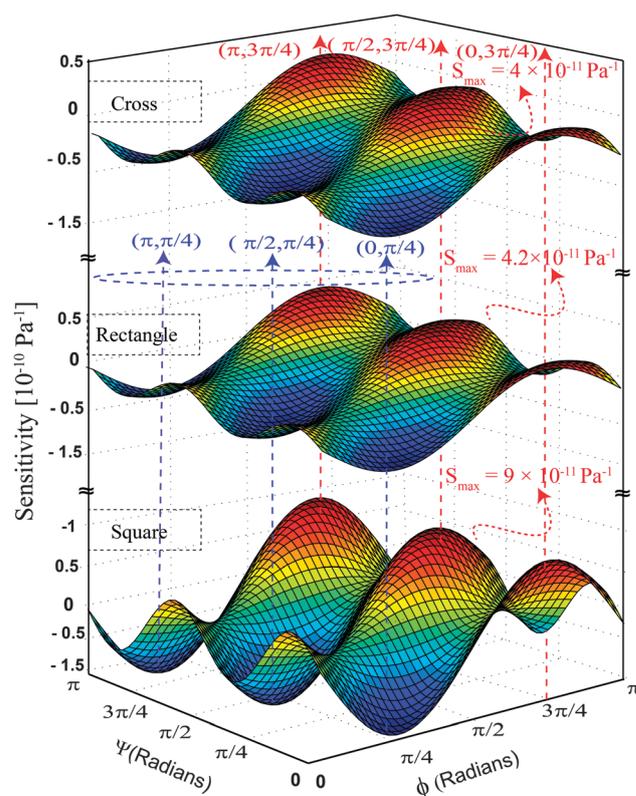


Fig. 8 Comparison of sensitivities of the different fabricated devices with variation of the crystal orientation and direction of stress:  $\Psi$  is the angle between the direction of current and the [100] crystal orientation,  $\phi$  is the angle between the direction of stress and the direction of current.

with respect to the (100) crystal plane. It is clear from Fig. 8 that the sensitivities of the each device depend not only upon the device geometry but also upon the directions of current and stress in the crystallographic plane. The square device has the maximum sensitivity of  $9.0 \times 10^{-11} \text{ Pa}^{-1}$  while the cross-device has maximum sensitivity of  $4.0 \times 10^{-11} \text{ Pa}^{-1}$  (Table 1) highlighted by the red arrows in Fig. 8. This indicates that the stress

**Table 1** Maximum and minimum sensitivities of all device geometries along particular directions of current and stress in the (100) crystal plane

Geometry	Value	Current direction	Stress direction	Sensitivity ( $10^{-11} \text{ Pa}^{-1}$ )
Cross	Max.	[100]	[110]	4.0
	Min.	[010]	[100]	$\approx 0$
Rectangle	Max.	[100]	[110]	4.2
	Min.	[010]	[100]	$\approx 0$
Square	Max.	[100]	[110]	9.0
	Min.	[010]	[100]	$\approx 0$

sensitivity of the device can be increased or decreased by 100% with alteration of the device geometry only. The square and cross-devices are fabricated within the same area of  $500 \mu\text{m} \times 500 \mu\text{m}$  but the difference in the sensitivities is more than 100% which accentuate the importance of choosing the appropriate device geometry for maximum sensitivity. The rectangular device, which occupies more area than the square and cross-devices has stress sensitivity which is comparable to that of the cross-device. The maximum absolute sensitivity ( $|S|$ ) of the device is achieved at the set of values  $[(\Psi, \phi) = (a\pi/2, (2b + 1)\pi/4); a \text{ and } b \text{ are integers}]$ . The red arrows in Fig. 8 corresponds to the the tensile stress having maximum positive stress sensitivities. Similarly, the maximum negative stress sensitivities highlighted by the blue arrows correspond to the compressive stress. So another important conclusion which can be drawn from Fig. 8 that the sensitivity of the each device changes its sign when the stress is changed from tensile to compressive. So the device can be used to determine the magnitude and direction of stress simultaneously.

In conjunction with the stress sensing applications, these devices are used for sensing the magnetic field and are called Hall sensors. For the use of these devices as magnetic field sensors it is desirable for these devices to have minimum stress related variations in the offset voltage, which can be incorporated into the Hall devices during packaging, absorption of moisture, deformation of the PCB and stresses introduced during application if used in a mechanical environment. So the analysis of the effect of device geometry on the stress sensitivity is also important for Hall sensors. As we can see from Fig. 8 that the stress related sensitivity of the offset voltage of the Hall device can be minimized by using a cross-device geometry which is 100% less sensitive to the square device. Similarly, the rectangular device also produces fewer offset errors in the offset voltage as compared to the square device. The direction of input current in the crystal plane also plays important role for the stress-dependent offset voltage of the Hall device and it must be chosen so as to have less stress sensitivity. The set of values of  $\Psi$  and  $\phi$  preferred for Hall devices can be chosen to be  $[(\Psi, \phi) = (a\pi/4, b\pi/2); a \text{ and } b \text{ are integers}]$ .

The analysis of the impact of device geometry on stress-dependent offset voltage of the four terminal devices has been presented in the (100) crystal plane. It has been observed that the device geometry plays a significant role in the stress sensitivity of the device. The sensitivity of the device can be

increased by almost 100% by selecting the optimum device geometry. The square device has been found to be an appropriate choice as a stress sensor and the cross-device is the optimum device geometry for magnetic field sensors to have minimum stress related offset variations. It has also been concluded that as the device is rotated within the (100) crystal plane the sensitivity of the device varies very significantly from  $\approx 0$  to  $9 \times 10^{-11} \text{ Pa}^{-1}$  as the direction of input current is varied in the (100) crystal plane. Both the device geometry and the direction of input current in the (100) crystal plane are very important for designing MEMS sensors for stress sensing applications and magnetic field sensors. Using the results obtained in this study the optimum device geometry and direction of current in the (100) crystal plane can be predicted for both stress sensors and magnetic field sensors.

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## References

- 1 G.-Y. Li, J. Ma, G. Peng, W. Chen, Z.-Y. Chu, Y.-H. Li, T.-J. Hu and X.-D. Li, *ACS Appl. Mater. Interfaces*, 2014, **6**, 22673.
- 2 M. Mehregany, C. A. Zorman, N. Rajan and C. H. Wu, *Proc. IEEE*, 1998, **86**, 1594.
- 3 R. Okojie, D. Lukco, V. Nguyen and E. Savrun, *IEEE Electron Device Lett.*, 2015, **36**, 174.
- 4 H. P. Phan, P. Tanner, D. V. Dao, N. T. Nguyen, L. Wang, Y. Zhu and S. Dimitrijević, *IEEE Electron Device Lett.*, 2014, **35**, 399.
- 5 H. P. Phan, D. V. Dao, P. Tanner, N. T. Nguyen, L. Wang, Y. Zhu and S. Dimitrijević, *Appl. Phys. Lett.*, 2014, **104**, 111905.
- 6 H. P. Phan, D. V. Dao, P. Tanner, N. T. Nguyen, J. S. Han, S. Dimitrijević, G. Walker, L. Wang and Y. Zhu, *J. Mater. Chem. C*, 2014, **2**, 7176–7179.
- 7 H. P. Phan, D. V. Dao, L. Wang, T. Dinh, N.-T. Nguyen, A. Qamar, P. Tanner, S. Dimitrijević and Y. Zhu, *J. Mater. Chem. C*, 2015, **3**, 1172–1176.
- 8 P. M. Sarro, *Sens. Actuators, A*, 2000, **82**, 210.
- 9 F. Gao, J. Zheng, M. Wang, G. Wei and W. Yang, *Chem. Commun.*, 2011, **47**, 11993.
- 10 J. Bi, G. Wei, L. Wang, F. Gao, J. Zheng, B. Tang and W. Yang, *J. Mater. Chem. C*, 2013, **1**, 4514.
- 11 R. Shao, K. Zheng, Y. Zhang, Y. Li, Z. Zhang and X. Han, *Appl. Phys. Lett.*, 2012, **101**, 233109.
- 12 T. Akiyama, D. Briand and N. F. Rooij, *J. Micromech. Microeng.*, 2012, **22**, 085034.
- 13 R. S. Okojie, A. A. Ned, A. D. Kurtz and W. N. Carr, *IEEE Trans. Electron Devices*, 1998, **45**, 785.

- 14 F. L. Via, M. Camarda and A. L. Magna, *Appl. Phys. Rev.*, 2014, **1**, 031301.
- 15 J. S. Shor, D. Goldstein and A. D. Kurtz, *IEEE Trans. Electron Devices*, 1993, **40**, 1093.
- 16 S. Roy, C. Jacob and S. Basu, *IEEE Trans. Electron Devices*, 2003, **94**, 298.
- 17 R. C. Jaeger, J. C. Suhling and R. Ramani, *IEEE Trans. Compon., Hybrids, Manuf. Technol.*, 1994, **17**, 97–107.
- 18 A. Mian, J. C. Suhling and R. Jaeger, *IEEE Sens. J.*, 2006, **6**, 340–356.
- 19 Y. Kanda, *Jpn. J. Appl. Phys.*, 1987, **26**, 1031.
- 20 A. V. Gridchin and V. A. Gridchin, *Sens. Actuators, A*, 1997, **58**, 219.
- 21 M. Doelle, D. Mager, P. Ruther and O. Paul, *Sens. Actuators, A*, 2006, **127**, 261.
- 22 R. Sunier, S. Taschini, O. Brand, T. Vancura, H. Baltesl, TRANSDUCERS, Solid-State Sensors, Actuators and Microsystems, 12th International Conference on, 2003, **2**, 1582.
- 23 Y. Kanda and M. Migitaka, *Phys. Status Solidi A*, 1976, **35**, K115.
- 24 Y. Kanda and A. Yasukawa, *Sens. Actuators*, 1982, **2**, 283.
- 25 Y. Kanda and K. Yamamura, *Sens. Actuators*, 1989, **18**, 247.
- 26 Y. Kanda and M. Migitaka, *Phys. Status Solidi A*, 1976, **38**, K41.
- 27 Y. Kanda, *Sens. Actuators*, 1983, **4**, 199.
- 28 D. V. Dao, T. Toriyama, J. Wells, S. Sugiyama, 2002 15th IEEE International Conference on MEMS. 2002; pp. 312–315.
- 29 J. C. Doll and B. L. Pruitt, *Piezoresistor design and applications*, Springer, New York, 2013.
- 30 J. Gragg, *Silicon pressure sensor, US Pat.*, 4317126, 1982.
- 31 L. Wang, S. Dimitrijevic, J. Han, P. Tanner, A. Lacopi and L. Hold, *J. Cryst. Growth*, 2011, **329**, 67–70.
- 32 A. Qamar, P. Tanner, D. V. Dao, H.-P. Phan and T. Dinh, *IEEE Electron Device Lett.*, 2014, **35**, 1293–1295.
- 33 A. Qamar, D. V. Dao, P. Tanner, H.-P. Phan, T. Dinh and S. Dimitrijevic, *Appl. Phys. Express*, 2015, **8**, 061302.
- 34 A. Qamar, H.-P. Phan, D. Dao, P. Tanner, T. Dinh, L. Wang and S. Dimitrijevic, *IEEE Electron Device Lett.*, 2015, **1**.